New accurate temperature dependent timing model in digital standard cell designs

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***Abstract*—This paper introduces a new temperature dependent timing model that allows designers to deal with accurate temperature dependent delays in logic simulations. In this proposal we present the latest enhancements in the CellTherm logi-thermal simulator developed in the Department of Electron Devices, BME, Hungary. With the proposed accurate temperature dependent timing model thermal effects affecting delays in digital standard cell integrated circuits can be modeled with delay-temperature functions. In order to establish the model preliminary delay-temperature characterization is needed for the standard cells building up the circuit. We propose the extension of the industry standard Liberty format developed by Synopsys with the new model. With the new accurate model we demonstrate that present temperature-timing models do not describe temperature dependent operation sufficiently. In our presented model timing and power data can be parameterized by temperature vectors. It is also demonstrated that taking temperature dependent delays into account allows for more precise power modeling that is critical in low-power nanometer integrated systems.**

I. Weaknesses of present timing models

The timing information of standard cells in today's integrated circuit design systems are stored in different databases. Most typically the timing and delay data of a standard cell library are stored in a Liberty database [1], [2] that circuit design applications use during synthesis and place&route (P&R). Logic simulators use the pre- or post-layout timing databases generated by the synthesizer applications for timing simulations. These timing data are usually stored in Standard Delay Files (SDF) [3]. The SDF files are generated by the synthesizer softwares during synthesis and P&R from the Liberty database. In the Liberty database, the delays and timing arcs of the standard cells are stored in a parametric form. This means that timing data in the Liberty file are characterized and stored for numerous input slew, load capacitance parameters. This way the synthesizer can calculate delays for the cells in the design according to the actual placement and routing. With each placement and routing scenario different SDF data are calculated for different layouts. This allows for accurate logic and timing simulations where actual layout topologies are taken into account.

The disadvantage of the mentioned timing model is that the cell libraries are characterized on previously established and fixed process, voltage and temperature (PVT) corners [4]–[6]. The characterized data are valid for those certain corners thus for other corners a re-characterization is needed. The Composite Current Source (CCS) model developed by Synopsys [1], [7] addresses the problem of voltage and process parameter scaling by storing current waveforms in the Liberty database [8] rather than derived quantities like power or energy. On the other hand, the CCS model neither takes ambient and self-temperature variations into account that is necessary for temperature dependent delay simulations. Neither the former Non-Linear Delay Model (NLDM) nor the Scalable Polynomial Delay Model take device temperatures accurately into account. These limitations mean that a re-characterization is needed for the cell library for each temperature corner.

With present models, delay changes caused by temperature variations can only be determined accurately at the characterized corners. On other temperatures delay values can be calculated with linear interpolation. However, cell delays calculated with linear interpolation can be inaccurate. More precise temperature dependence of delays can be achieved by characterizing delays in a wide temperature range with sufficient resolution (e.g. 1 °C).

By characterizing the cell library for a wide temperature range with high resolution more precise timing and logi-thermal simulation results can be achieved. Timing, switching activity, power and temperature depend mutually on each other, since with varying delays switching activity changes in a unit time slot, that causes the change of dynamic power consumption that affects device temperature. Moreover, changing temperature modifies timing.

In this paper we propose a new timing model in which we characterize propagation delays in a standard cell library in a wide temperature range with high resolution. The temperature dependent delays of the cells can be taken into consideration by the characterized *delay-temperature* curves. With the proposed model the thermal behavior of a standard cell design can be described precisely.

The presented model can be easily integrated into the Liberty database which can effectively store multi-dimensional functions.

II. Generation and description of the new model

We describe the creation of the new model step-by-step. Figure 1. helps the comprehension of the model generation flow.

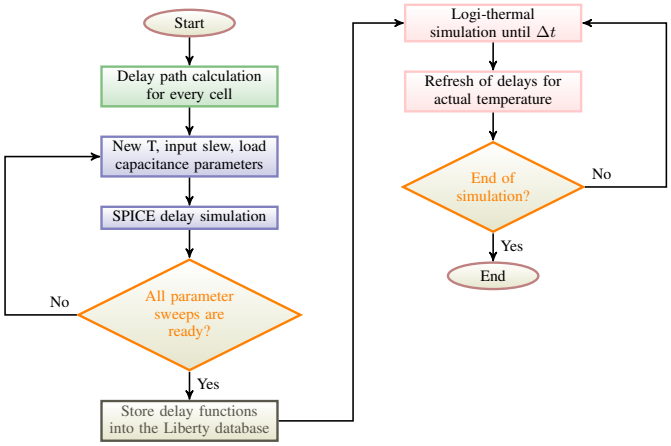

Fig. 1. Model generation steps

1) For the generation of the model the delay paths of each cell must be known. Propagation delays can be defined for these paths. In a cell as many delays can be defined as the number of input-output paths. For example, in a two input, one output NAND gate there are two paths between the inputs and the output. Temperature dependent delays must be calculated for each possible paths. The mentioned timing paths need not to be determined by hand as the cell library usually contains a behavioral description of the cells in either Verilog or VHDL code and these often define the paths. In absence of these behavioral descriptions the plain logic and timing simulation would not be possible either.
2) The precise temperature dependent delays can be calculated with analog SPICE simulations in possession of the transistor level netlists of the cells. We have used the ELDO analog simulator from Mentor Graphics that contains built-in functions to determine propagation delays. For example, an inverter's propagation delay can be extracted with the `.EXTRACT TRAN VECT TPD(V(A), V(Y))` command. During the analog simulation the cell's temperature change can be simulated by sweeping the ambient temperature. For each delay path one delay value is calculated for one temperature.
   For the delay-temperature curves the ambient temperature should be swept in a wide range with fine resolution. This way for each temperature a new delay value is calculated. Precision can be controlled by the sampling density of the sweep. With the ELDO simulator any parameter value can be easily swept with built-in commands. For example, the `.STEP TEMP -20 85 1` instructs the simulator to sweep the ambient temperature from $-20\,°C$ to $85\,°C$ in $1\,°C$ steps.
   Propagation delay is not only dependent on the temperature but also on the input signal slew and output load capacitance. Thus the delay-temperature functions should be parameterized with these values. Using ELDO's parameter sweep feature (`.STEP` command) it is easy to create measurements which calculate propagation delays for every temperature, input slew and output load value. This process results in 4-dimensional tables that can be stored for the logi-thermal simulation. Figure 2. shows an example for such a table.

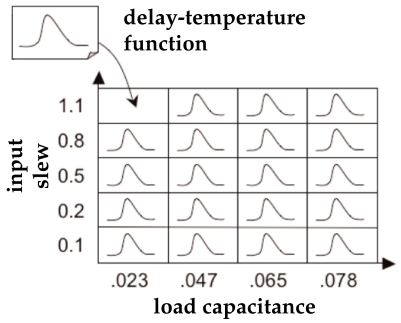

Fig. 2. Delay-temperature functions in the Liberty format

   The multi-dimensional data can be effectively stored in a Liberty database along with the CCS current functions of the cells.
3) After the analog simulations, results should be stored in the Liberty database. The logi-thermal simulator will extract the temperature dependent delays from this database in every thermal time step (Δt).
4) The CellTherm logi-thermal simulator [9], [10] calculates the temperature distribution on the chip in each Δt time step. Using the delay-temperature functions it extracts the delays according to the current temperatures of the cells. This iteration is done until the simulation ends.

With the classic SDF delay model delays can be defined for only *three* temperature corners. These corners are referred to with *minimum*, *typical* and *maximum* terms henceforth. With the SDF model delays can be specified between the three temperature corners with linear interpolation. Extrapolation can be used beyond the corners. Because of using interpolation the calculated delays could differ significantly from the real temperature dependent delays. The difference between the two models is depicted in figure 3.

SDF_{min}, SDF_{typ} and SDF_{max} values stand for the *minimum*, *typical* and *maximum* temperature corners and their corresponding delay values. In these points the SDF delay values are equal to the accurate temperature dependent delays. The accurate characterization is done between T_{min} and T_{max} temperatures. It is visible that the presented accurate model describes the temperature dependent delays more precisely. With the 3-corner interpolation the SDF model could cause a significant error in logic timing during the logi-thermal simulation. With the proposed new timing model cell delays can be defined for arbitrary number of temperatures.

III. Demonstration of the Model

We demonstrate our new timing model on a simple ring oscillator circuit. The schematic of the ring oscillator is shown

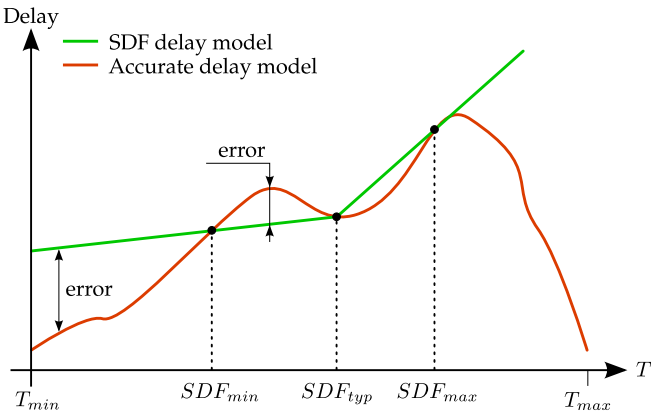

Fig. 3. Comparison of the new and classic models

in figure 4. The circuit contains 10 inverter cells and a kick-in NAND gate.

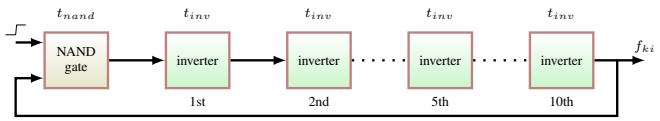

Fig. 4. Schematic of the ring oscillator

The output frequency of the oscillator can be calculated with (1) if the inverter delays are assumed the same.

$$f_{out} = \frac{1}{2 \cdot (t_{nand} + 10 \cdot t_{inv})}, \tag{1}$$

where t_{nand} is the NAND gate's delay, t_{inv} is the delay of the inverters and f_{out} is the output frequency of the ring oscillator.

Our proposed timing model is compared with the interpolated delays of the classic SDF model. By running the same logi-thermal simulations on both models we prove the advantages of the new temperature dependent timing model over the classic SDF delay calculations. In this demonstration the input signal slews and output load capacitances are locked on reasonable values for simplicity and lucidity.

The temperature dependent delays of the cells have to be prepared before the simulation. The creation of these functions can be done simultaneously with other characterizations of the cell library such as power and timing measurements. The characterization is usually done by the silicon foundry that provides the process design kit (PDK) to the users. According to our proposal the temperature dependent delay functions can also be shipped with the PDK by integrating them into the Liberty database.

IV. Delay-temperature functions

In the presented demonstration the ambient temperature was swept in the range of $-20\,°C$ to $85\,°C$. The SPICE characterization was done for the cells of the ring oscillator circuit, namely the NAND gate and the inverters. The delay-temperature functions measured with the SPICE simulations are shown in figures 5 and 6. Similar delay-temperature curves are shown in [11].

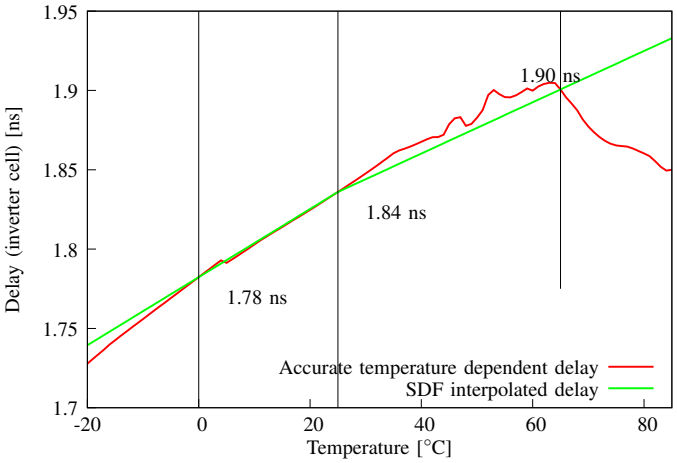

Fig. 5. Delay-temperature functions of the inverter cells

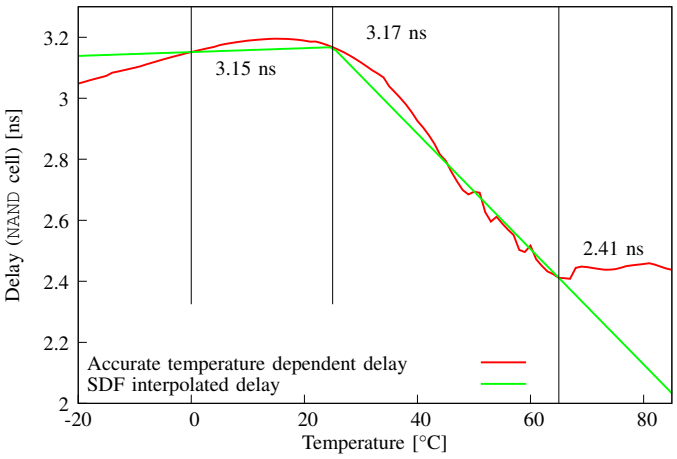

Fig. 6. Delay-temperature functions of the NAND cell

Temperature dependence represented by the classic SDF model is also depicted on figures 5 and 6. In the SDF model the delay values are characterized on $0\,°C$, $25\,°C$ and $65\,°C$. The intermediate delay values can be calculated by linear interpolation. It is noticeable that as the piecewise linear SDF function diverges from the characterization corners the error rises with respect to the accurate delay-temperature functions.

V. Logi-thermal simulation based on SDF delays

The logi-thermal simulation was run on the demonstration circuit with both the classic SDF delays and the proposed new timing model. In both cases the simulation was run for $4\,s$. This time was enough for the circuit to reach a steady thermal state with both models.

First, the logi-thermal simulation was run with the classic SDF delay model. Figure 7 shows the thermal transient function of the `inv5` inverter cell. In the demonstrated circuit the temperature difference between the cells was negligible compared to the overall temperature thus the temperature of the `inv5` cell will be the reference henceforward.

It is shown in figure 7 that the circuit heats up to 70 °C at 0 °C ambient temperature. By observing figures 5 and 6 it is obvious that over 65 °C the SDF interpolated delays differ significantly from the real temperature dependent delays.

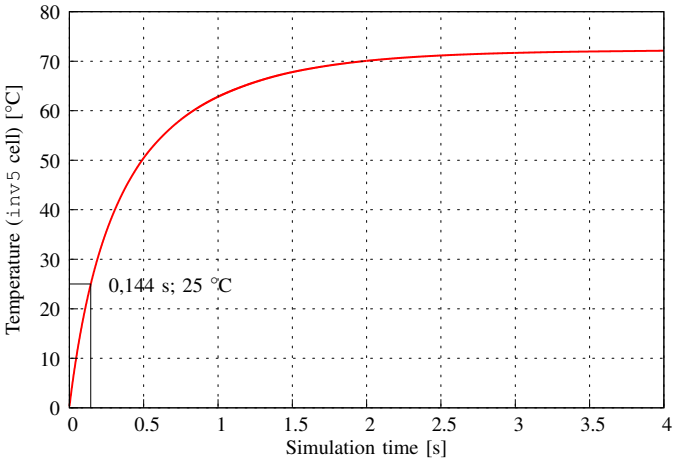

Fig. 7. Thermal transient of the `inv5` cell

In figure 7 the time where the circuit reaches 25 °C is marked. This point is interesting because the classic SDF delay model has the sole breakpoint at this temperature. This means that abrupt change in delay values are expected at this temperature. The `inv5` cell reached 25 °C in 0.144 s.

Simulation result made with the classic SDF model is shown in figure 8. The output period of the ring oscillator is depicted in the figure. For lucidity and comparability the function shows only the oscillator output period versus simulation time. Output frequency can be calculated from the reciprocal of the period.

In figure 8 it is observable that the output period changes abruptly at 0.144 s. This is caused by the breakpoint in the SDF piecewise linear model at 25 °C. Figure 8 shows a spectacular example of how errors are introduced by linear approximation of real temperature dependent delays. The oscillator output period versus the temperature of the `inv5` cell is shown in figure 9. The linear nature of the period-temperature function is obvious because of the linear delay-temperature functions in the SDF model. Figure 9 shows two curves, the simulation result and a calculated period.

In order to validate the simulation results the output period over temperature was also calculated analytically. From the SDF piecewise linear delay functions the oscillator output period can be calculated. In the SDF delay database, the inverter delays are the same for simplicity. Apart from the inverter delays, the kick-in `NAND` gate's delays are given in

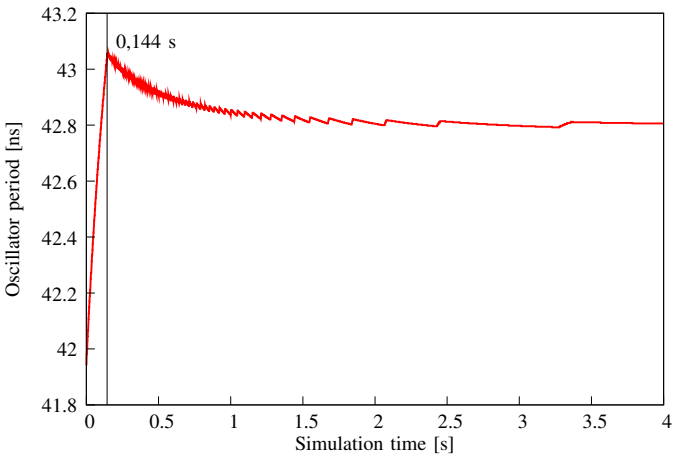

Fig. 8. Period measured with SDF delays

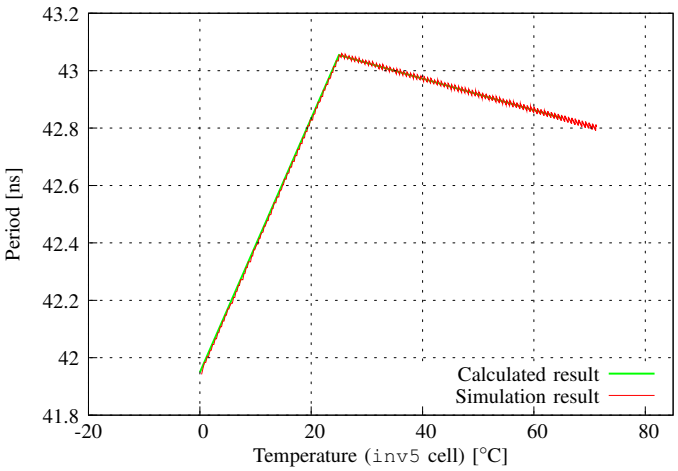

Fig. 9. Period in function of `inv5` cell's temperature

the SDF file. The resulting output period can be calculated from these values with (2).

$$t_{\text{period}} = 2 \cdot (t_{nand} + 10 \cdot t_{inv}), \tag{2}$$

where t_{nand} is the `NAND` gate's delay and t_{inv} is the delay of inverters. In figure 9 it is visible that the calculated and simulated output period functions are the same.

VI. Logi-thermal simulation based on accurate delay-temperature functions

The logi-thermal simulation presented in section V has also been executed with the accurate temperature dependent delay model proposed in this paper. The output period over simulation time is shown in figure 10.

It is noticeable in figure 10 that the output period function is much more detailed than those simulated with the classic SDF model. The output period function has also been measured in function of the temperature. This is depicted in figure 11.

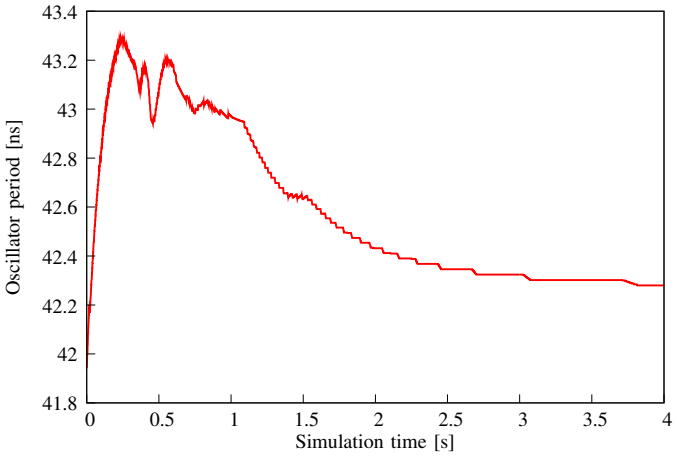

Fig. 10. Period simulated with accurate delay-temperature functions

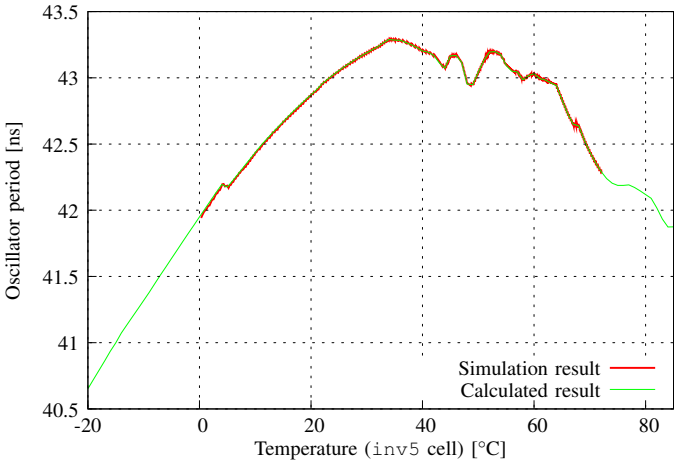

Fig. 11. Period versus temperature simulated with accurate delays

The analytic calculation of the output period was also done for our proposed accurate temperature dependent delay model with (2). Figure 11 shows both the calculated and the simulated waveform of the output period versus temperature. It is noticeable that the calculation and simulation results match here as well. It is also observable that the simulated function is valid in the 0 °C to 72 °C range because the circuit's overall temperature stays in this range. The calculated function, due to the characterization range, falls in the −20 °C to 85 °C range.

VII. Comparison of the Models

By comparing the simulation results of the classic SDF model and the accurate temperature dependent timing model it can be stated that more precise and accurate logi-thermal simulation results can be achieved with our new proposed timing model. Therefore careful characterization of delays in function of temperature is a critical and important step before logi-thermal simulations. There is significant difference in resolution and accuracy between the classic SDF and our proposed model. Differences of the two models can be best emphasized and visualized with the simulation results shown in a combined diagram in figure 12.

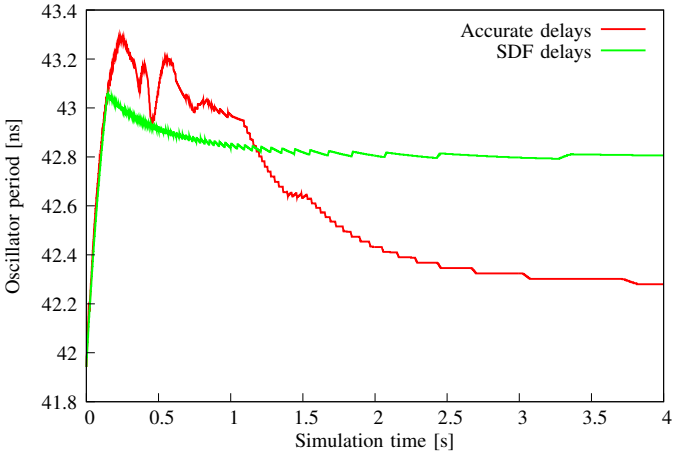

Fig. 12. Comparison in function of time

It is observable that there is significant difference between the two curves. By using the accurate temperature dependent model the output period curve does not change abruptly at 25 °C. The exact shape of the period functions is determined by the NAND and inverter cells' delay-temperature characteristics together. The delay of the NAND cell is greater than the inverter's delay (see figures 5 and 6) but the ten inverter's accumulated delay dominates. In this example the inverse temperature dependence (ITD) [12]–[16] of the delay characteristics is also conspicuous. Due to the ITD effect it is possible that the cell delays decrease with rising temperatures. This means that device speed increases with rising temperatures. This phenomenon is also noticeable in our accurate model simulations. The oscillator's output period starts to increase with increasing temperature under 35 °C. Over 35 °C, output period decreases so output frequency increases. At thermal steady state the circuit will operate on a slower frequency than the initial, but the difference between the output periods in the two extrema cannot be accurately simulated with the classic piecewise SDF delay model. In figure 13 the output period for both models is shown with respect to device temperature.

The delays depending on the device temperature also affect the dissipated power because switching activity in a time slot depends on cell delays. This influences dynamic dissipation. With our presented accurate model thermally induced dissipation changes can also be detected and simulated. With logi-thermal simulations the dissipation changes can be implicitly simulated and temperature variations caused by power fluctuations can be detected. Resulting dissipation difference of the classic SDF and the proposed accurate models is shown in figure 14.

In figure 14 it is observable that there is clearly a difference between the simulated dissipations of the SDF and the proposed model.

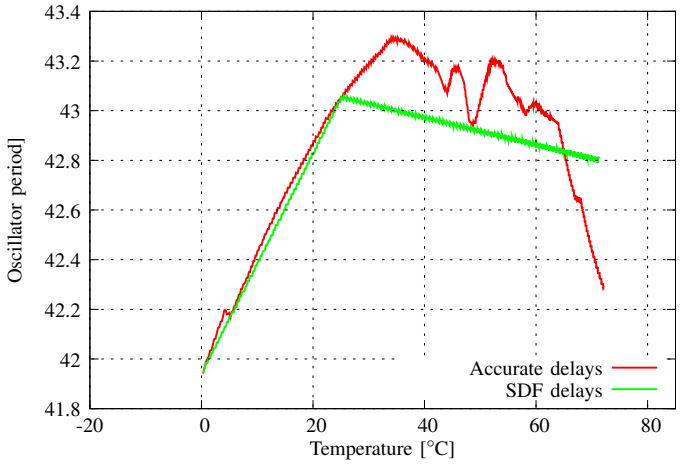

Fig. 13. Comparison in function of temperature

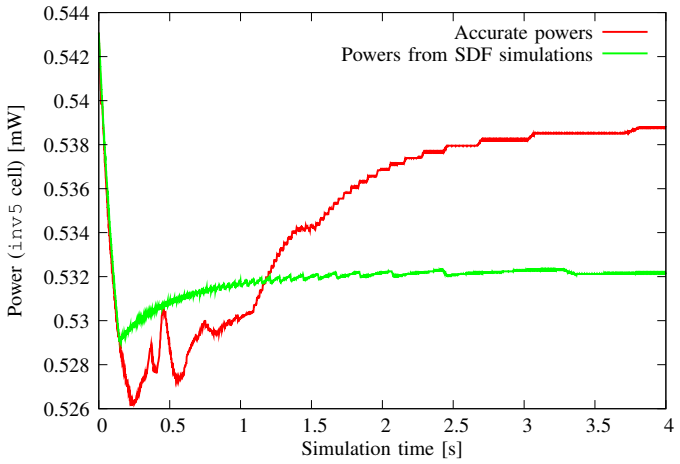

Fig. 14. Dissipation differences

VIII. Extension of the Liberty format

Precise temperature dependent delays characteristics have to be stored for every cell in the design. The open standard Liberty format developed by Synopsys [1] allows usage of user-defined attributes and groups to enhance and extend the format. The Liberty format is suitable to store multi-dimensional functions effectively. The database stores power, timing and noise data in tables indexed by different parameters. The standardized Liberty format also provides a parser API that can be used in third party applications to extract data from these databases. The CellTherm logi-thermal simulator uses this API to get data from Liberty files. According to our proposal the precise temperature dependent delay functions can also be stored in this database. This allows usage of the current API to extract the temperature dependent delays from the Liberty data.

To store user-defined functions in the Liberty database the format has to be extended by custom storage groups and attributes. By defining these new properties in language level it is assured that the parser API can read the user-defined data.

IX. Summary

In this paper we presented a new temperature dependent delay model for digital standard cell integrated circuits. The model uses delay-temperature functions of the library cells that need to be characterized during creation of the process design kit. The characterized delay-temperature functions can be stored in the open standard Liberty format processed by synthesis and place and route applications. We have demonstrated that delay dependence on temperature cannot be accurately modeled with present standard delay formats like SDF. Our proposed accurate temperature-aware timing model takes varying temperatures across the chip surface and provides access to temperature dependent delays for logi-thermal simulations. The presented accurate model is used in the CellTherm logi-thermal simulator developed in the Department of Electron Devices, BME, Hungary. It is also demonstrated that taking temperature dependent delays into account allows for more precise power modeling that is critical in low-power nanometer integrated systems.

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